W83781D/W83781G

WINBOND
H/W MONITORING IC

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1. GENERAL DESCRIPTION

The W83781D/G is a hardware monitoring IC for personal computers, server computers, or microprocessor based systems. W83781D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stablely and properly. W83781D provides both ISA and I^2C^{TM} serial bus interface.

A 8-bit analog-to-digital converter (ADC) was built inside W83781D/G. The W83781D/G can monitor 3 external thermistor temperature sensors, 5 positive analog voltage inputs, two inverting inputs (for monitoring negative voltages), and also three fan tachometer outputs. There is also one input for case open detection circuits.

With the application software, the users can read all the monitored parameters of system from time to time. The application software could be the popular Intel™ LDCM (LANDesk Client Management) or Winbond application software. Also the users can set up the upper and lower limits of these monitored parameters and to activate two programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters is out of the preset range.

Additionally, 5 VID inputs are provided to read the VID of CPU (such as Pentium™ II) if applicable. This is to provide the Vcore correction automatically. Also W83781D uniquely provides an optional feature: early stage (before BIOS was load) beep warning. This is to detect if the fatal elements present --- VcoreA, +3.3V voltage fail, and the system can not be boomed up.

2. FEATURES

2.1 Monitoring Items

- 3 thermal inputs from remote thermistors
- 5 positive voltage inputs (typical for +12V, +5V, +3.3V, VcoreA, VcoreB)
- 2 op amps for negative voltage monitoring (typical for -12V, -5V)
- 3 fan speed monitoring inputs
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items

2.2 Actions Enabling

- Warning signal pop up in application software
- Beep tone warning
- Fan ON/OFF control
- Issue SMI#, IRQ to activate system protection

2.3 General

- ISA and I²C™ serial bus interface
- 5 VID input pins for CPU Vcore identification
- Initial power fault beep (for +3.3V, VcoreA)
- Master reset input to W83781D/G
- Independent power plane of digital Vcc and analog Vcc (input to IC)
- Intel LDCM™ compatible
- Winbond monitoring application software support
- Input clock rate optional for 24, 48, 14.318 MHz

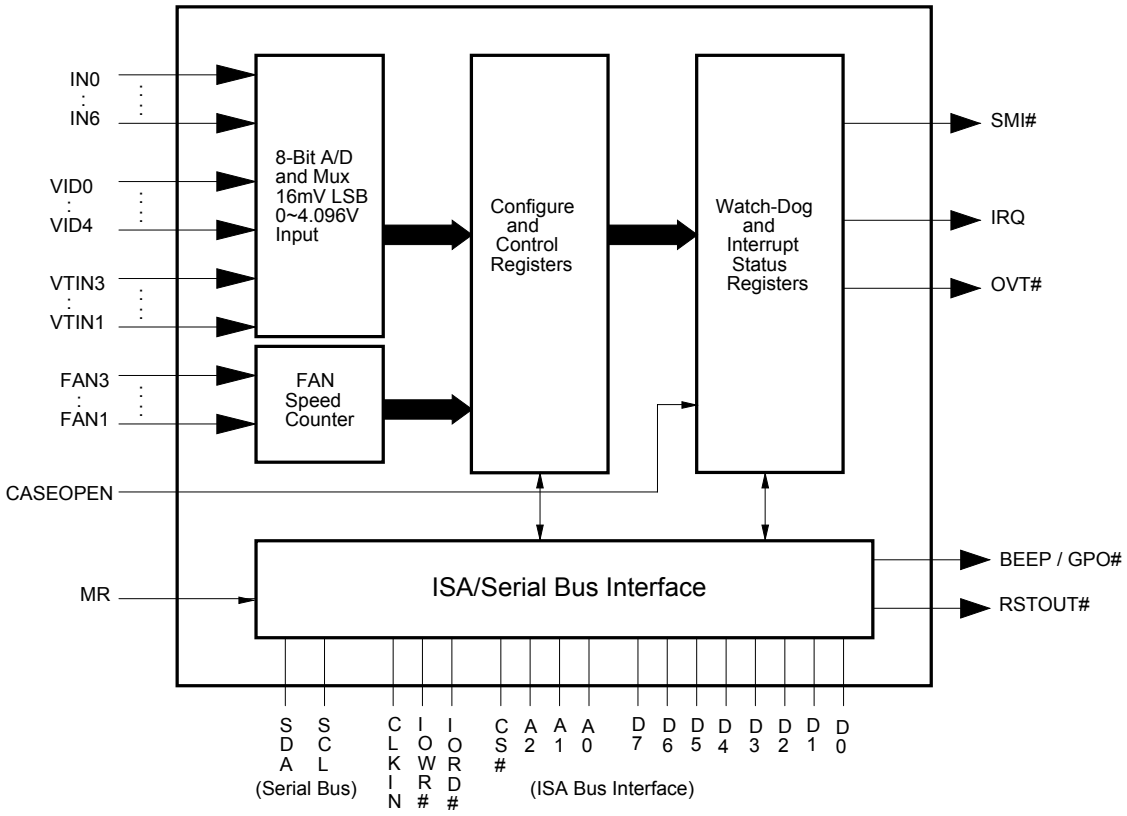
2.4 Package

- 48-pin LQFP

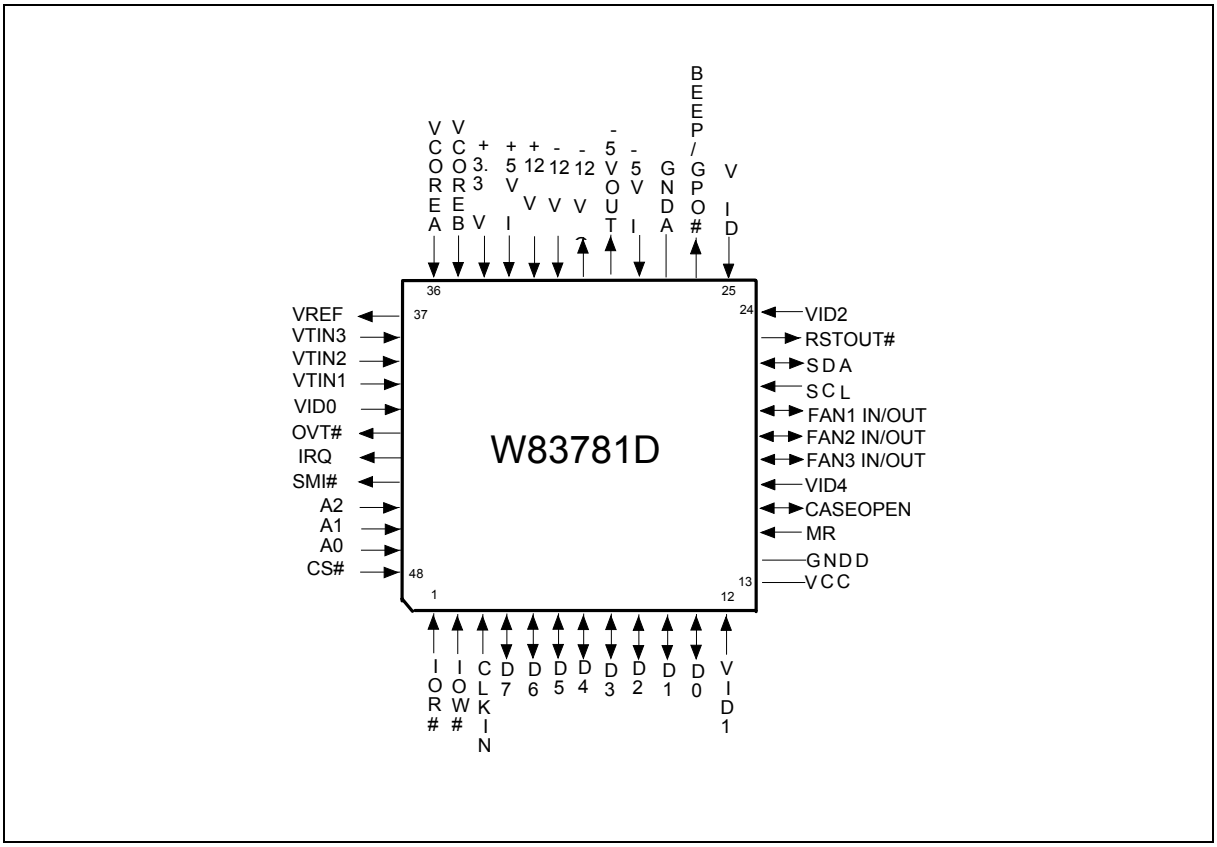
3. KEY SPECIFICATIONS

• Voltage monitoring accuracy	±1% (Max)
• Monitoring Temperature Range and Accuracy	
- 40°C to +120°C	± 3°C(Max)
• Supply Voltage	5V
• Supply Current	Operating: 1 mA typ.
	Shutdown: 10 μA typ.
• ADC Resolution	8 Bits

4. BLOCK DIAGRAM



5. PIN CONFIGURATION



6. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

OUT_{12t} - TTL level output pin with 12 mA source-sink capability

OUT_{8t} - TTL level output pin with 8 mA source-sink capability

AOUT - Output pin(Analog)

OD_8 - Open-drain output pin with 8 mA sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{48} - Open-drain output pin with 48 mA sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
IOR#	1	IN_{ts}	An active low standard ISA bus I/O Read Control.
IOW#	2	IN_{ts}	An active low standard ISA bus I/O Write Control.
CLKIN	3	IN_{t}	System clock input. Can select 48MHz or 24MHz or 14.318MHz. The default is 24MHz.
D7~D0	4-11	I/O_{12t}	Bi-directional ISA bus Data lines. D0 corresponds to the low order bit, with D7 the high order bit.
VID1	12	IN_{t}	Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register.
V_{CC} (+5V)	13	POWER	+5V V_{CC} power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
GNDD	14	DGROUND	Internally connected to all digital circuitry.
MR	15	IN_{ts}	Master reset input.
CASEOPEN	16	I/O_{12t}	CASE OPEN. An active high input from an external circuit which latches a Case Open event. This line can go high without any clamping action intrusion regardless of the powered state of the W83781D/G. The W83781D/G provides an internal open drain on this line, controlled by Bit 7 of IRQ Mask Register 2, to provide a minimum 20 ms reset of this line.
VID4	17	IN_{t}	Voltage Supply readouts from P6.This value is read in the bit <0> of Device ID Register.
FAN3-FAN1 IN/OUT	18-20	I/O_{12ts}	0V to +5V amplitude fan tachometer input / Fan on-off control output. These multifunctional pins can be programmable input or output.
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	I/O_{12ts}	Serial Bus bi-directional Data.
RSTOUT#	23	OUT_{8t}	8 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 7 in SMI# Mask Register 2.
VID2	24	IN_{t}	Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register.
VID3	25	IN_{t}	Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register.
BEEP/GPO#	26	OD_{48}	Beep function or General purpose output (active low). This pin is open drain driving 48 mA. This multifunctional pin is programmable selected by CR4D bit 6.
GNDA	27	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN	28	AIN	Ground-referred inverting op amp input.
-5VOUT	29	AOUT	Output of inverting op amp for Input 6.
-12VOUT	30	AOUT	Output of inverting op amp for Input 5.

Continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
-12VIN	31	AIN	Ground-referred inverting op amp input.
+12VIN	32	AIN	0V to 4.096V FSR Analog Inputs.
+5VIN	33	AIN	This pin is Analog Vcc and connects internal monitor channel IN3 with fixed scale.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
VCOREB	35	AIN	0V to 4.096V FSR Analog Inputs.
VCOREA	36	AIN	0V to 4.096V FSR Analog Inputs.
VREF	37	AOUT	Reference Voltage.
VTIN3	38	AIN	Thermistor 3 terminal input.
VTIN2	39	AIN	Thermistor 2 terminal input.
VTIN1	40	AIN	Thermistor 1 terminal input.
VID0	41	IN_t	Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register.
OVT#	42	OD_{12}	Over temperature Shutdown Output.
IRQ	43	OUT_{12t}	Interrupt Request.
SMI#	44	OD_{12}	System Management Interrupt (open drain). This output is enabled when Bit 1 in the Configuration Register (CR40) is set to 1. The default state is disabled.
A2-A0	45-47	IN_t	The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds to the lowest order bit.
CS#	48	IN_t	Chip Select input from an external decoder which decodes high order address bits on the ISA Address Bus. This is an active low input.

# Indicates Active Low("Not")

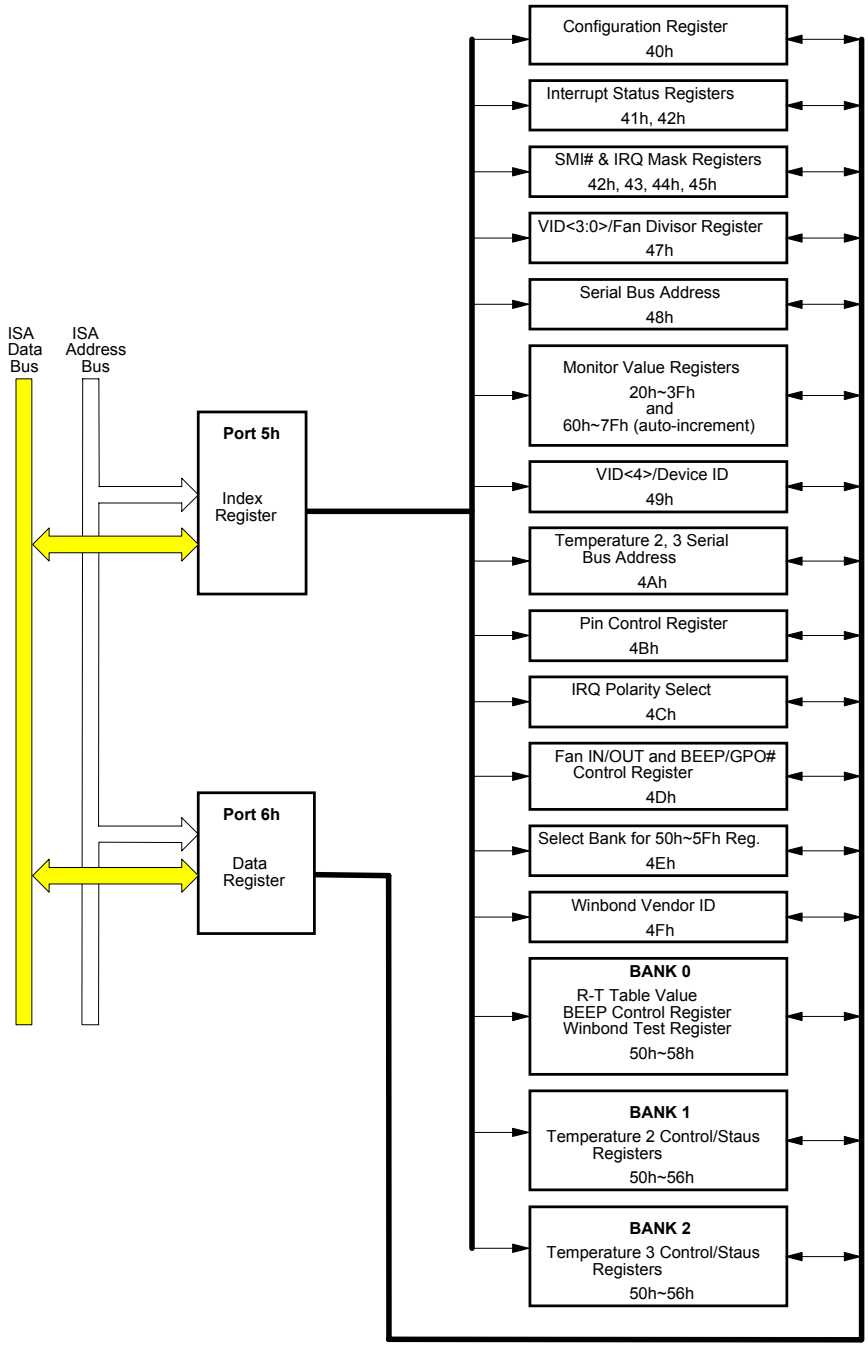
7. FUNCTIONAL DESCRIPTION

7.1 General Description

The W83781D/G provides 5 analog positive inputs, 2 analog negative input, 3 fan speed monitors or fan ON/OFF control, 3 thermistor voltage inputs, case open detection and beep function output when the monitor value exceed the set limit value. When start the monitor function on the chip, the watch dog machine monitor every function and store the value to registers. If the monitor value exceeds the limit value, the interrupt status will be set to 1.

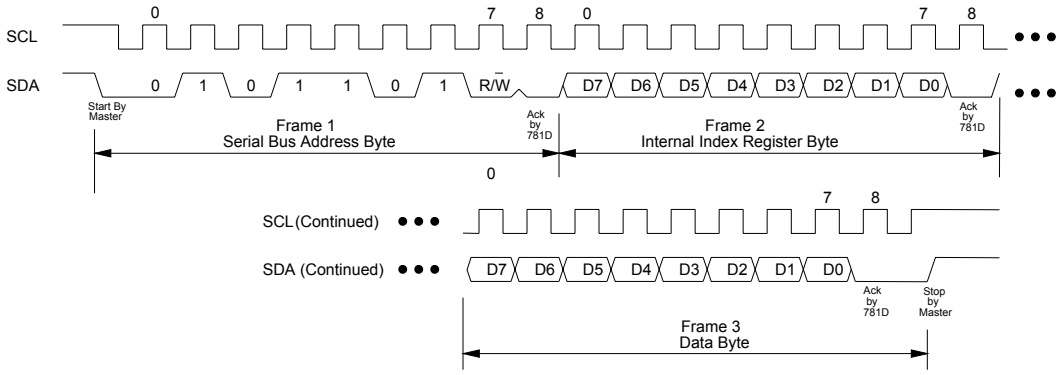
The W83781D/G provides two interface for microprocessor to read/write internal registers. The first interface use ISA Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The high byte of these ports is decoded by Chip Select (CS#), the general decoded address is set to port 295h and port 296h. These two ports are described as following:
Port 295h: W83781D/G Index register port.
Port 296h: Data port.

The register structure is showed as the diagram next page.
The second interface use Serial Bus. In the W83781D/G has three serial bus address. That is, the first address defined at CR48 can read/write all registers excluding Bank 1 and Bank 2 temperature 2/3 registers, the second address defined at CR4A.bit2-0 only read/write temperature sensor 2 registers, and the third address defined at CR4A.bit6-4 only can access (read/write) temperature sensor 3 registers.



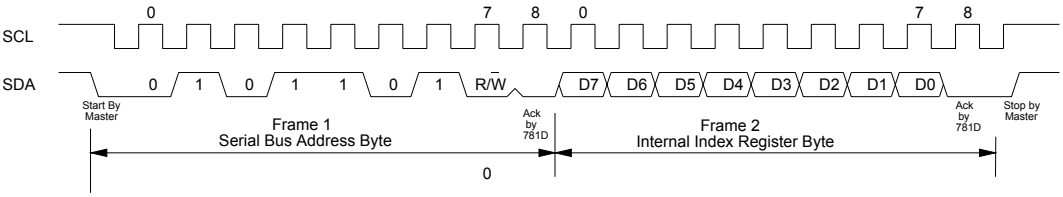
7.1.1 The first serial bus access timing is shown as follows:

(a) Serial bus write to internal address register followed by the data byte



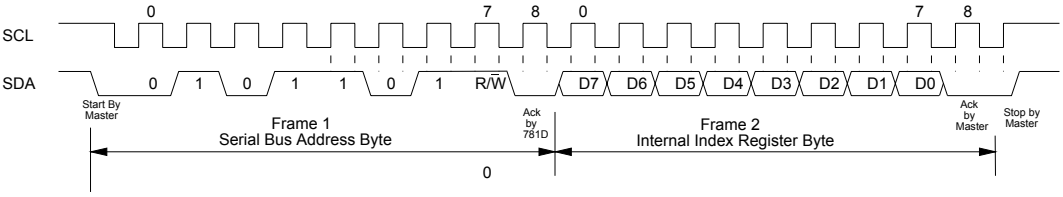
Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus **write** to internal address register only



Serial Bus Write to Internal Address Register Only

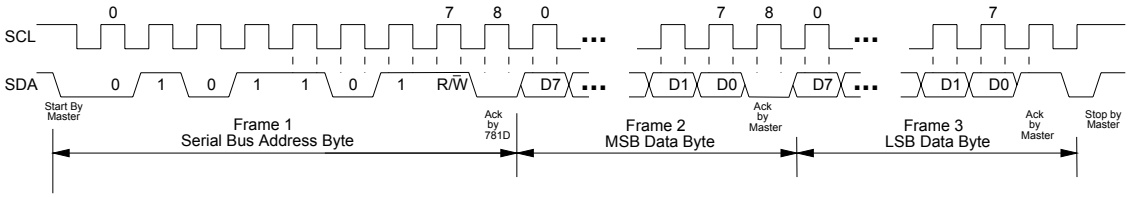
(c) Serial bus **read** from a register with the internal address register prefer to desired location



Serial Bus Write to Internal Address Register Only

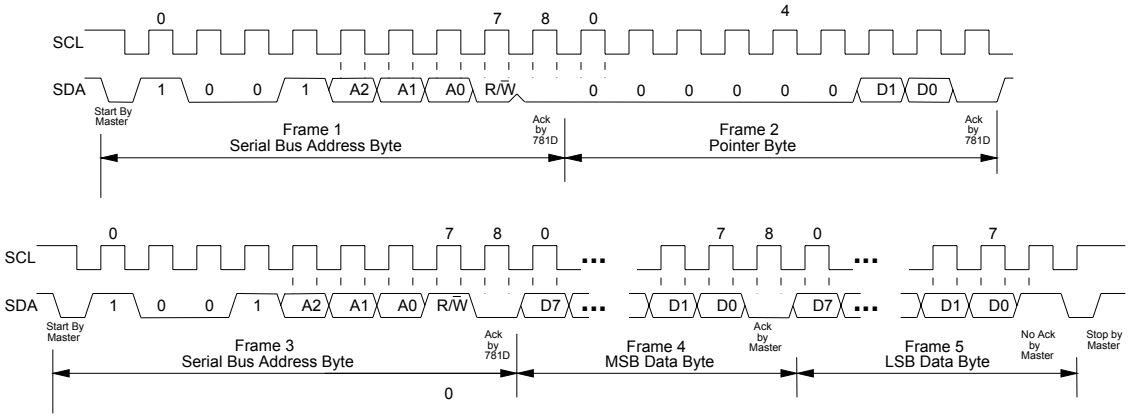
7.1.2 The serial bus timing of the temperature 2 and 3 is shown as follows:

(a) Typical **2-byte read** from preset pointer location (Temp, T_{OS}, T_{HYST})



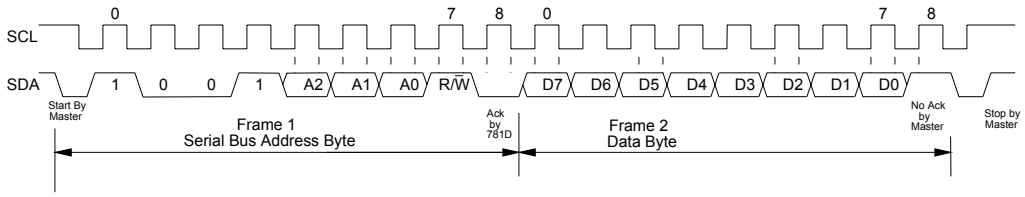
Typical 2-Byte Read From Preset Pointer Location

(b) Typical pointer set followed by immediate **read** for **2-byte register** (Temp, T_{OS}, T_{HYST})



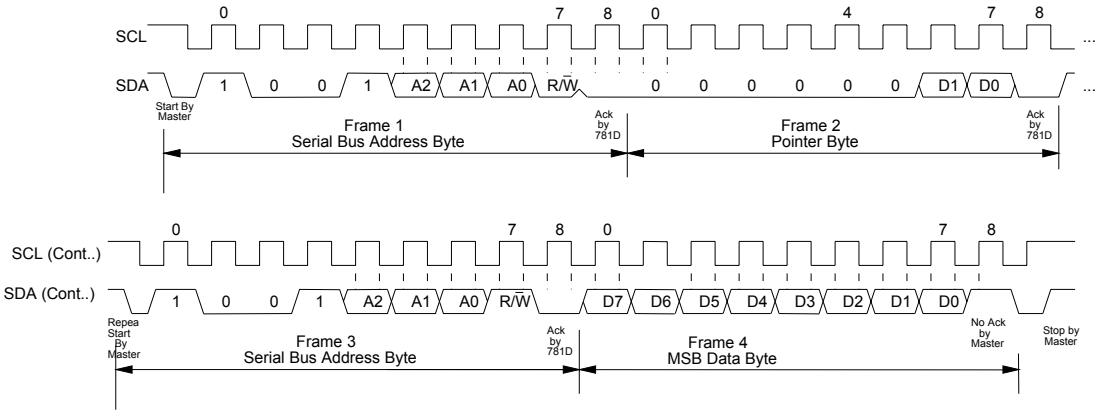
Typical Pointer Set Followed by Immediate Read for 2-Byte Register

(c) Typical **read 1-byte** from configuration register with preset pointer



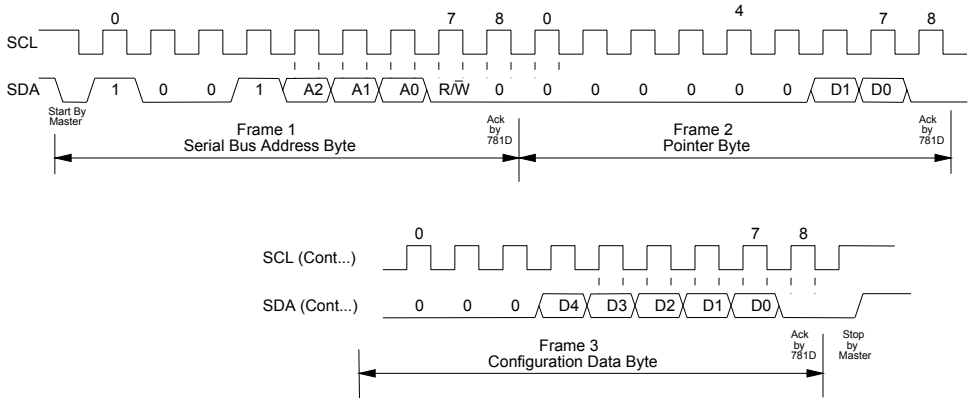
Typical 1-Byte Read From Configuration With Reset Pointer

(d) Typical pointer set followed by immediate **read** from **configuration register**



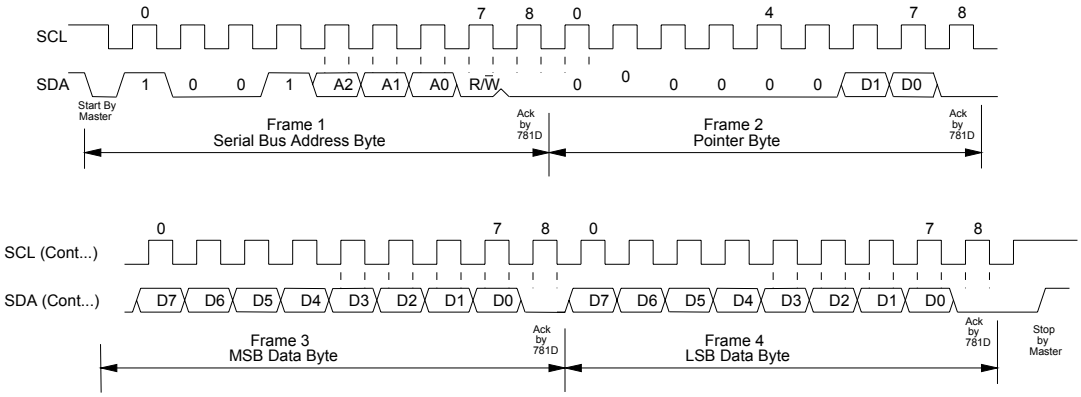
Typical Pointor Set Followed by Immediate Read from Temp 2/3 Configuration Register

(e) Temperature 2/3 configuration register **Write**



Configuration Register Write

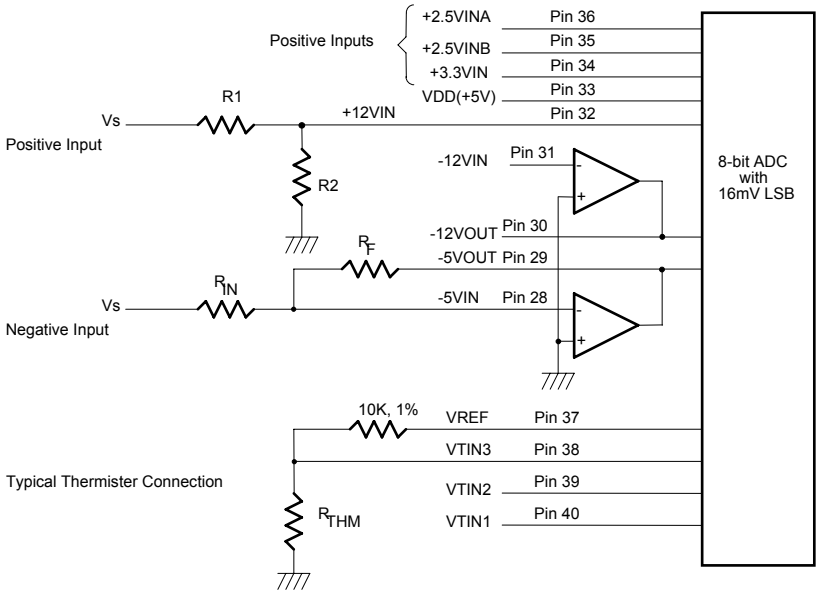
(f) Temperature 2/3 T_{OS} and T_{HYST} **write**



Configuration Register Write

7.2 Analog Inputs

The maximum input voltage of the analog pin is 4.096 because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage and 3.3V can directly connected to these analog inputs. The +5V and +12V inputs should be reduced a factor with external resistors so as to obtain the input range. As followed figure is shown.



The input voltage can be expressed as following equation.

$$V_{IN} = V_s \times \frac{R_2}{R_1 + R_2}$$

The value of R_1 and R_2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage is 12V. The Pin 33 is connected to +5V power supply to provide analog power, and this voltage is connected to internal resistors to monitor the +5V voltage.
The negative voltage should be connected an op amps to invert and reduce the -5V and -12V voltage. The input voltage can be calculated by following equation.

$$V_S = -V_{IN} \times (\frac{R_F}{R_{IN}})$$

The Winbond recommended value is R_{IN}=90.9K Ohms and R_F=60.4K Ohms for -5V voltage input, R_{IN}=210K Ohms and R_F=60.4K Ohms for -12V voltage input.
The temperature sensors are connected by a 10K Ohms, then connect to VREF (Pin 37). The sensors should choose 10K Ohms at 25°C and β-value is 3435 for default R-T table. If the β-value is not 3435, the R-T table should be re-program to generate a correct temperature.

7.3 FAN Inputs and FAN Control

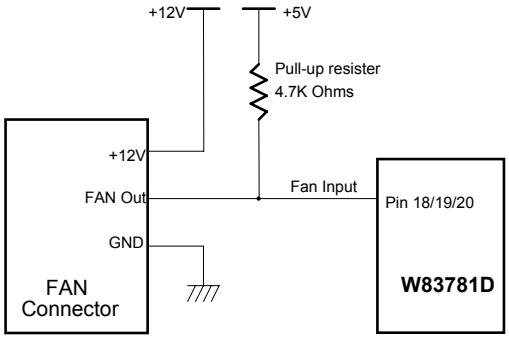
Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as following.

Determine the fan counter according to:

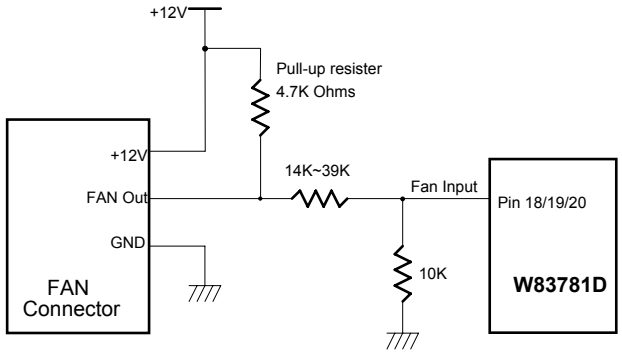
$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

The default divisor is 2 and defined at CR47.bit7~4 and CR4B.bit7~6. The followed table is an example for the relation of divisor, PRM, and count.

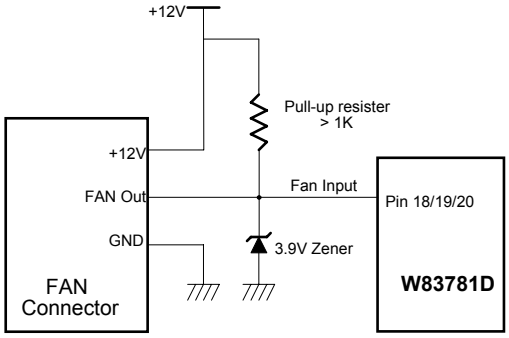
DIVISOR	NOMINAL PRM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.74 ms
2	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms



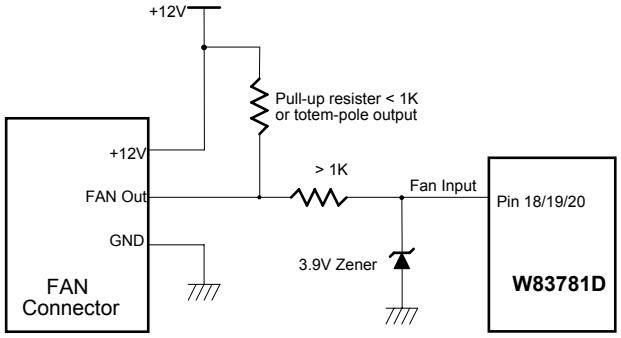
Fan with Tach Pull-Up to +5V



Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator



Fan with Tach Pull-Up to +12V and Zener Clamp



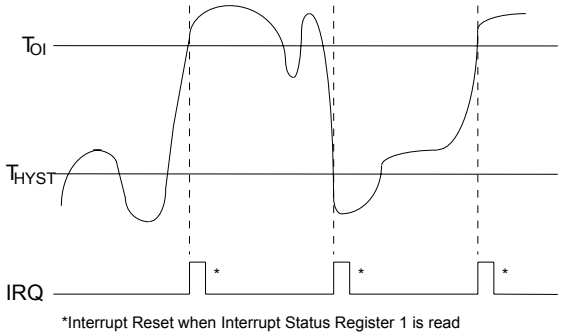
Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

7.4 Temperature Measurement Machine

The temperature data format is 8-bit two -complement for sensor 1 and 9-bit two -complement for sensor 2/3. The table are expressed the temperature data as following.

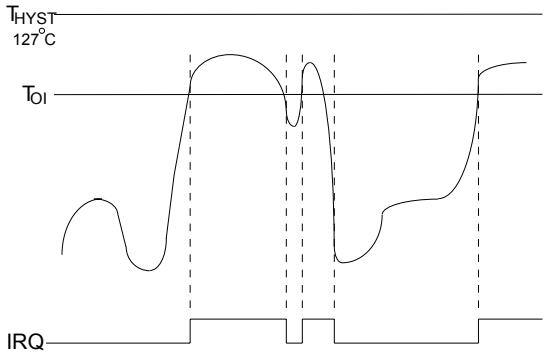
Temperature	8-Bit Digital Output		9-Bit Digital Output	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

The W83781D/G temperature interrupt has two mode: (1) The first is Interrupt Mode--exceeding T_{OI} causes an interrupt until reset by reading Interrupt Status Register 1 (CR41). Once an interrupt event has occurred over T_{OI}, the interrupt will occur again by the temperature going below T_{HYST}. (2) Comparator Mode--setting the T_{HYST} limit to 127°C will cause the comparator mode. When temperature exceeds T_{OI}, the interrupt will be generate Interrupt. If the temperature goes below the T_{OI}, the interrupt will be reset. Two interrupt modes are shown as below.



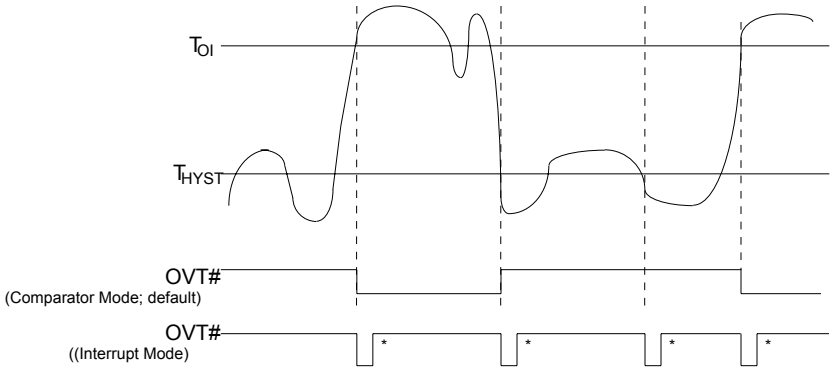
*Interrupt Reset when Interrupt Status Register 1 is read

(1) Interrupt Mode



(2) Comparator Mode

The temperature sensor 2 or 3 Over-Temperature (OVT) response is same as temperature sensor 1 IRQ signal.



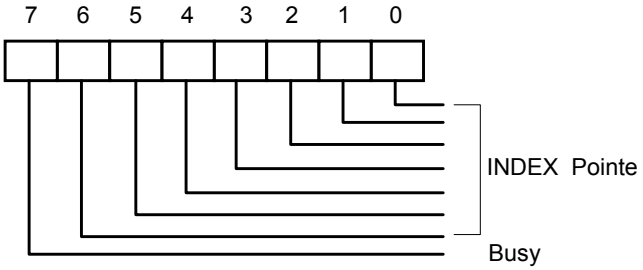
*Interrupt Reset when Temperature 2/3 is read

Over-Temperature Response Diagram

8. CONTROL AND STATUS REGISTERS

8.1 Address Register (Port x5h)

The main register is the INDEX Register located at Port x5h. The bit designations are as follows:



Bit7: Read Only

The logical 1 indicates the device is busy because of a Serial Bus transaction or another ISA bus transaction. With checking this bit, multiple ISA drivers can use W83781D/G without interfering with each other or a Serial Bus driver.

It is the user's responsibility not to have a Serial Bus and ISA bus operations at the same time.

This bit is:

Set: with a write to Port x5h or when a Serial Bus transaction is in progress.

Reset: with a write or read from Port x6h if it is set by a write to Port x5h, or when the Serial Bus transaction is finished.

Bit 6-0: Read/Write

INDEX of Control and Status Registers. See the tables below for detail.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Busy	Index Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

Index Pointer (A6-A0)

Registers	Bank	A6-A0 in Hex	Power On Value of Registers: <7:0>in Binary	Notes
Configuration Register	0	40h	00001000	
Interrupt Status Register 1	0	41h	00000000	Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h.
Interrupt Status Register 2	0	42h	00000000	

Index Pointer (A6-A0), continued

Registers	Bank	A6-A0 in Hex	Power On Value of Registers: <7:0>in Binary	Notes
SMI# Mask Register 1	0	43h	00000000	Auto-increment to the address of SMI# Mask Register 2 after a read or write to Port x6h.
SMI# Mask Register 2	0	44h	00000000	
IRQ Mask Register 1	0	45h	00000000	Auto-increment to the address of IRQ Mask Register 2 after a read or write to Port x6h
IRQ Mask Register 2	0	46h	00000000	
VID/Fan Divisor Register	0	47h	<7:4> = 0101; <3:0> = VID3-VID0	
Serial Bus Address Register	0	48h	<6:0> = 0101101; <7> = 0	
Voltage ID	0	49h	<7:6> is Reserved <5:4> is 01 binary <0> is mapped to VID <4>	
Temperature 2 and Temperature 3 Serial Bus Address Register	0	4Ah	<7:0> = 0000,0001 binary	
Pin Control Register	0	4Bh	<7:0> 44h	
RQ/OVT# Property Select	0	4Ch	<7:0> ---0,0001	
FAN IN/OUT and BEEP/GPO# Control Register	0	4Dh	<7:0> 0001,0101	
Register 50h ~ 5Fh Bank Select	0	4Eh	<6:3> = Reserved, <7> = 1, <2:0> = 0	
Winbond Vendor ID	0	4Fh	<15:0> = 5CA3h	
Resistor-Temperature Table Register	0	50-51h		
FAN Input Clock Pre-Divisor Register 2	0	55h	<7:0> -000,0001	
BEEP Control Register 1	0	56h	<7:0> 0000,0000	
BEEP Control Register 2	0	57h	<7:0> 1000-0000	

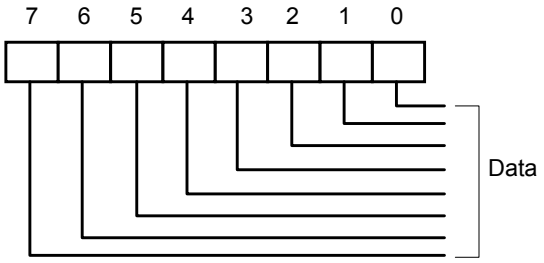
Index Pointer (A6-A0), continued

Registers	Bank	A6-A0 in Hex	Power On Value of Registers: <7:0>in Binary	Notes
Chip ID	0	58h	<7:0> 0001-0000	
Temperature Sensor 2 Temperature Register	1	50-51h		
Temperature Sensor 2 Configuration Register	1	52h	<7:0> = 0x00	
Temperature Sensor 2 Hysteresis (High Byte) Register	1	53h	<7:0> = 0x4B	
Temperature Sensor 2 Hysteresis (Low Byte) Register	1	54h	<7:0> = 0x0	
Temperature Sensor 2 Over-temperature(High Byte) Register	1	55h	<7:0> = 0x50	
Temperature Sensor 2 Over-temperature (Low Byte) Register	1	56h	<7:0> = 0x0	
Temperature Sensor 3 Temperature Register	2	50-51h		
Temperature Sensor 3 Configuration Register	2	52h	<7:0> = 0x00	
Temperature Sensor 3 Hysteresis (High Byte) Register	2	53h	<7:0> = 0x4B	
Temperature Sensor 3 Hysteresis (Low Byte) Register	2	54h	<7:0> = 0x0	
Temperature Sensor 3 Over-temperature (High Byte)Register	2	55h	<7:0> = 0x50	
Temperature Sensor 2 Over-temperature (Low Byte) Register	2	56h	<7:0> = 0x0	
Value RAM	0	20-3Fh		
Value RAM	0	60-7Fh		Auto-increment to the next location after a read or write to Port x6h and stop at 7Fh.

Note: Index Pointer (A6-A0) and Value RAM only can be read at the accurate bank.

8.2 Data Register (Port x6h)

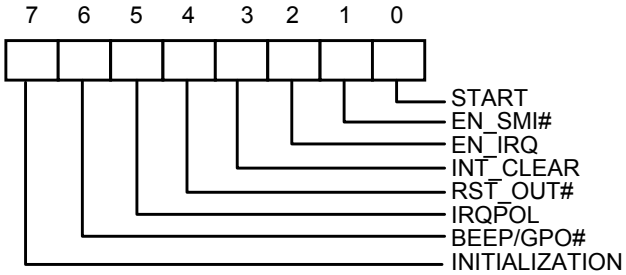
Data Port: Port x6h
Power on Default Value 00h
Attribute: Read/write
Size: 8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

8.3 Configuration Register – Index 40h (*Bank 0*)

Register Location: 40h
Power on Default Value 00000001 binary
Attribute: Read/write
Size: 8 bits



Bit 7: The logical 1 restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.

Bit 6: The logical 1 in this bit drives a zero on GPO# pin.

Bit 5: IRQ polarity select. When set to 0, IRQ active high. Set to 1, IRQ active low. Default 0.

Bit 4: The logical 1 outputs at least a 20 ms active low reset signal at RST_OUT# if <7> = 1 in SMI# Mask Register 2. This bit is cleared once the pulse has gone inactive.

Bit 3: The logical 1 disables the SMI# and IRQ outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: The logical 1 enables the IRQ Interrupt output.

Bit 1: The logical 1 enables the SMI# Interrupt output.

Bit 0: **1** enables startup of monitoring operations

0 puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_CLEAR" bit.

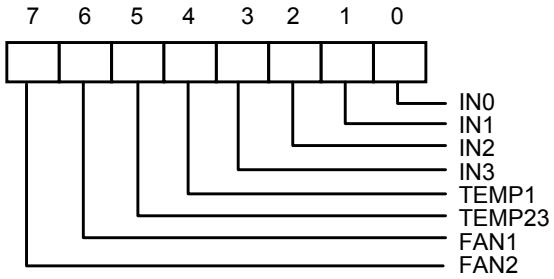
8.4 Interrupt Status Register 1 – Index 41h (*Bank 0*)

Register Location: 41h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7: The logical 1 indicates the fan count limit has been exceeded.

Bit 6: The logical 1 indicates the fan count limit has been exceeded.

Bit 5: The logical 1 indicates a High or Low limit has been exceeded from temperature sensor 2 or sensor 3. The high and low limits value are defined in index registers: 53h-56h of the Bank 1.

Bit 4: The logical 1 indicates a High or Low limit has been exceeded from temperature sensor 1.

Bit 3-0: The logical 1 indicates a High or Low limit has been exceeded.

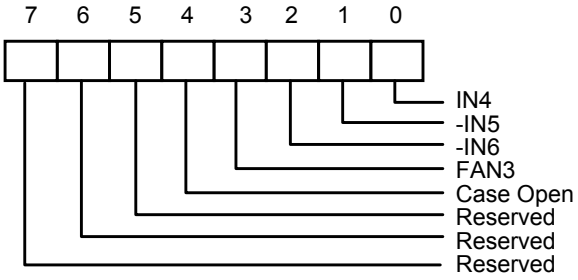
8.5 Interrupt Status Register 2 – Index 42h (*Bank 0*)

Register Location: 42h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7-5: Reserved.This bit should be set to 0.

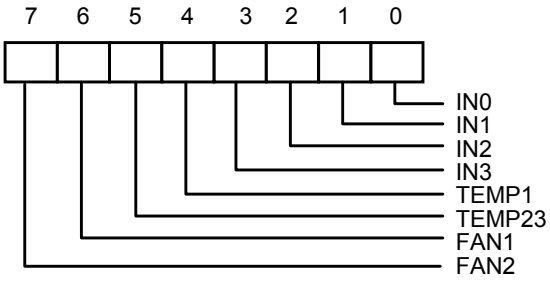
Bit 4: The logical 1 indicates Case Open has gone high.

Bit 3: The logical 1 indicates the fan count limit has been exceeded.

Bit 2-0: The logical 1 indicates a High or Low limit has been exceeded.

8.6 SMI# Mask Register 1 – Index 43h (*Bank 0*)

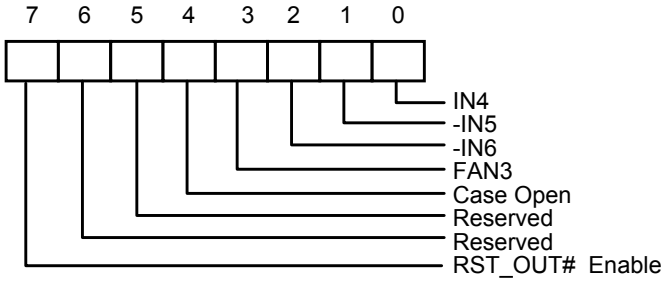
Register Location: 43h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: The logical 1 disables the corresponding interrupt status bit for SMI# interrupt.

8.7 SMI# Mask Register 2 – Index 44h (*Bank 0*)

Register Location: 44h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



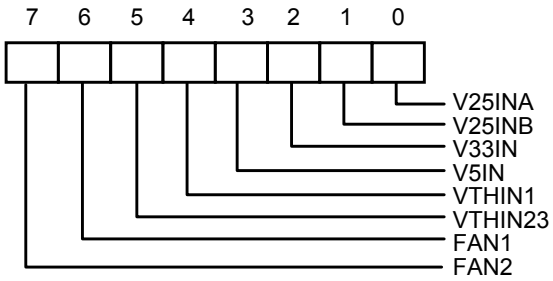
Bit 7: <7> = 1 in SMI# ask Register 2 enables the RST_OUT# in the Configuration Register. 13.8 IRQ Mask Register 1—Index 45h

Bit 6-5: Reserved. This bit should be set to 0.

Bit 4-0: The logical 1 disables the corresponding interrupt status bit for SMI# interrupt.

8.8 IRQ Mask Register 2 – Index 45h (*Bank 0*)

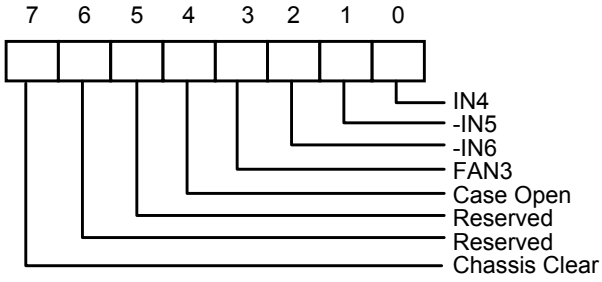
Register Location: 45h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: The logical 1 disables the corresponding interrupt status bit for IRQ interrupt.

8.9 IRQ Mask Register 2 – Index 46h (*Bank 0*)

Register Location: 46h
Power on Default Value <7:0> = 01000000 binary
Attribute: Read/Write
Size: 8 bits



Bit 7: The logical 1 outputs a minimum 20 ms active low pulse on the Case Open pin. The register bit self clears after the pulse has been output.

Bit 6-5: Reserved. This bit should be set to 0.

Bit 4-0: The logical 1 disables the corresponding interrupt status bit for IRQ interrupt.

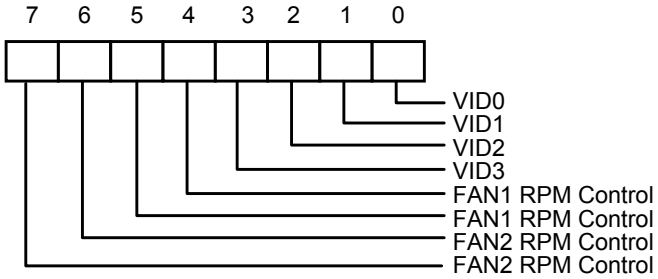
8.10 VID/Fan Divisor Register – Index 47h (*Bank 0*)

Register Location: 47h

Power on Default Value <7:4> is 0101, <3:0> is 0000

Attribute: Read/Write

Size: 8 bits



Bit 7-6: FAN2 Speed Control.

<7:6> = 00 - divide by 1;
<7:6> = 01 - divide by 2;
<7:6> = 10 - divide by 4;
<7:6> = 11 - divide by 8.

Bit 5-4: FAN1 Speed Control.

<5:4> = 00 - divide by 1;
<5:4> = 01 - divide by 2;
<5:4> = 10 - divide by 4;
<5:4> = 11 - divide by 8.

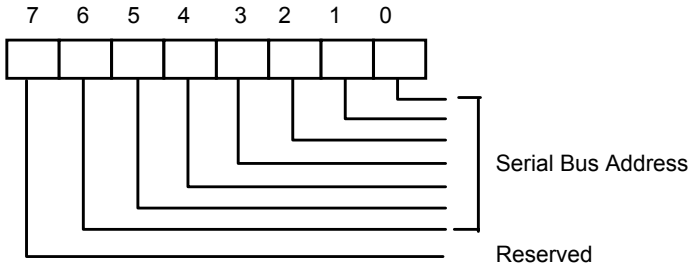
Bit 3-0: The VID <3:0> inputs

8.11 Serial Bus Address Register – Index 48h *(Bank 0)*

Register Location: 48h

Power on Default Value Serial Bus address <6:0> = 0101101 and <7> = 0 binary

Size: 8 bits



Bit 7: Read Only - Reserved.

Bit 6-0: Read/Write - Serial Bus address <6:0>.

8.12 Value RAM – Index 20h - 3Fh or 60h - Index 7Fh (auto-increment) (*Bank 0*)

INDEX A6-A0	INDEX A6-A0 WITH AUTO-INCREMENT	DESCRIPTION
20h	60h	IN0 reading
21h	61h	IN1 reading
22h	62h	IN2 reading
23h	63h	IN3 reading
24h	64h	IN4 reading
25h	65h	-IN5 reading
26h	66h	-IN6 reading
27h	67h	Temperature reading
28h	68h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	69h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	6Ah	FAN3 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Bh	6Bh	IN0 High Limit, default value is defined by Vcore Voltage +0.2V.

Value RAM — Index 20h- 3Fh or 60h – Index 7Fh (auto-increment) (*Bank 0*), continued

INDEX A6-A0	INDEX A6-A0 WITH AUTO-INCREMENT	DESCRIPTION
2Ch	6Ch	IN0 Low Limit, default value is defined by Vcore Voltage - 0.2V.
2Dh	6Dh	IN1 High Limit, , default value is defined by Vcore Voltage +0.2V.
2Eh	6Eh	IN1 Low Limit, default value is defined by Vcore Voltage - 0.2V.
2Fh	6Fh	IN2 High Limit
30h	70h	IN2 Low Limit
31h	71h	IN3 High Limit
32h	72h	IN3 Low Limit
33h	73h	IN4 High Limit
34h	74h	IN4 Low Limit
35h	75h	-IN5 High Limit
36h	76h	-IN5 Low Limit
37h	77h	-IN6 High Limit
38h	78h	-IN6 Low Limit
39h	79h	Over Temperature Limit (High)
3Ah	7Ah	Temperature Hysteresis Limit (Low)
3Bh	7Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	7Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	7Dh	FAN3 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3E- 3Fh	7E- 7Fh	Reserved

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

Note1: For the high limits of the voltages, the device is doing a greater than comparison. For the low limits, however, it is doing a less than or equal comparison.

Note 2: V-Core Table:

Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin					Vcore	Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin					Vcore
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
0	1	1	1	1	*	1	1	1	1	1	No CPU
0	1	1	1	0	*	1	1	1	1	0	2.1
0	1	1	0	1	*	1	1	1	0	1	2.2
0	1	1	0	0	*	1	1	1	0	0	2.3
0	1	0	1	1	*	1	1	0	1	1	2.4
0	1	0	1	0	*	1	1	0	1	0	2.5
0	1	0	0	1	*	1	1	0	0	1	2.6
0	1	0	0	0	*	1	1	0	0	0	2.7
0	0	1	1	1	*	1	0	1	1	1	2.8
0	0	1	1	0	*	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

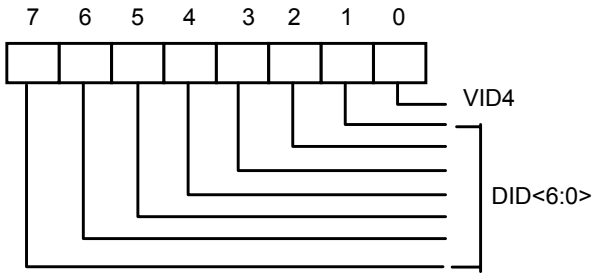
8.13 Voltage ID (VID7-4) – Index 49h (*Bank 0*)

Register Location: 49h

Power on Default Value <7:1> is 000, 0001b

<0> is mapped to VID <4>

Size: 8 bits



Bit 7-1: Read Only - Device ID<6:0>

Bit 0: Read/Write - The VID4 inputs/outputs. Reset by MR.

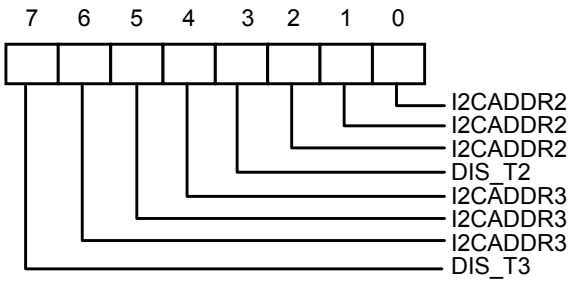
8.14 Temperature 2 and Temperature 3 Serial Bus Address Register Index 4Ah *(Bank 0)*

Register Location: 4Ah

Power on Default Value <7:0> = 0000, 0001 binary. Reset by MR

Attribute: Read/Write

Size: 8 bits

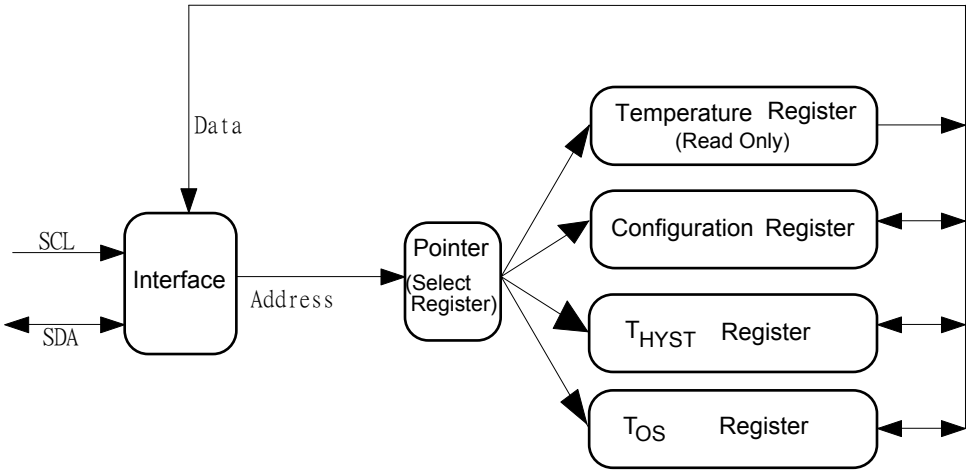


Bit 7: Set to 1, disable temperature sensor 3 and can not access any data from Temperature Sensor 3.

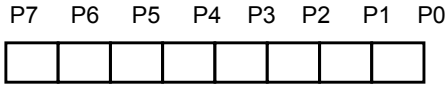
Bit 6-4: Temperature 3 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

Bit 3: Set to 1, disable temperature Sensor 2 and can not access any data from Temperature Sensor 2.

Bit 2-0: Temperature 2 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.



(Select which register will be read from or written to):

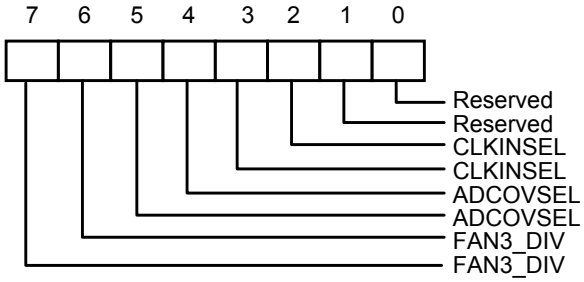


P7-P2: Must be kept 0.
P1-P0: Register select:

P1	P0	Index Register Selection (Bank1 & Bank2)	
0	0	Temperature (Read only) (Power up default)	CR50h & CR51h
0	1	Configuration (Read / Write)	CR52h
1	0	T_{HYST} (Read / Write)	CR53h & CR54h
1	1	T_{OS} (Read / Write)	CR55h & CR56h

8.15 Pin Control Register – Index 4Bh (*Bank 0*)

Register Location: 4Bh
Power on Default Value <7:0> 44h. Reset by MR.
Attribute: Read/Write
Size: 8 bits



Bit 7-6:Fan3 speed divisor.

<1:0> = 00 - divide by 1;<1:0> = 01 - divide by 2;
<1:0> = 10 - divide by 4;<1:0> = 11 - divide by 8;Reset by MR.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default.
<5:4> = 01- divided by 4.
<5:4> = 10 - divided by 16.
<5:4> = 11 - divided by 64.

Bit 3-2: Clock Input Select.

<3:2> = 00 - Pin 3 (CLKIN) select 14.318M Hz clock.
<3:2> = 01 - Default. Pin 3 (CLKIN) select 24M Hz clock.
<3:2> = 10 - Pin 3 (CLKIN) select 48M Hz clock .
<3:2> = 11 - Reserved. Pin3 no clock input.

Bit 1-0: Reserved. User defined.

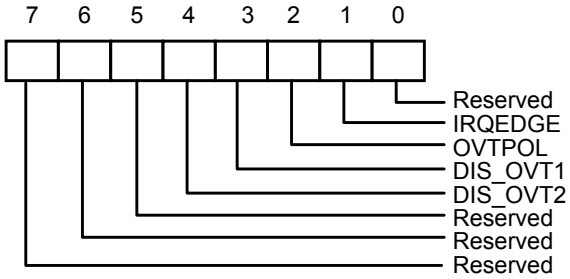
8.16 IRQ/OVT# Property Select – Index 4Ch (*Bank 0*)

Register Location: 4Ch

Power on Default Value <7:0> ---0,0001. Reset by MR.

Attribute: Read/Write

Size: 8 bits



Bit 7-5: Reserved. User Defined.

Bit 4: Disable temperature sensor 3 over-temperature (OVT) output if set to 1. Default 0, enable OVT2 output through pin OVT#.

Bit 3: Disable temperature sensor 2 over-temperature (OVT) output if set to 1. Default 0, enable OVT1 output through pin OVT#.

Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

Bit 1: When set to 1, IRQ Edge Active. Set to 0, IRQ Level trigger. Default 0, level trigger interrupt.

Bit 0: Reserved. User Defined.

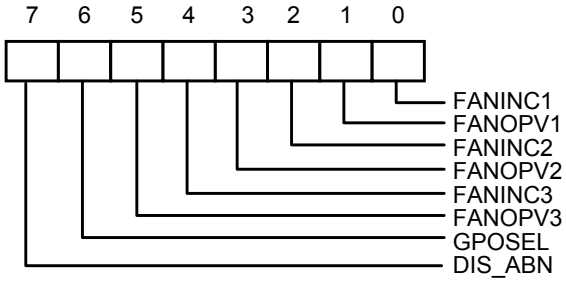
8.17 FAN IN/OUT and BEEP/GPO# Control Register – Index 4Dh (*Bank 0*)

Register Location: 4Dh

Power on Default Value <7:0> 0001,0101. Reset by MR.

Attribute: Read/Write

Size: 8 bits



Bit 7: Disable power-on abnormal the monitor voltage including V-Core A,, and +3.3V. If these voltage exceed the limit value, the pin (Open Drain) of BEEP will drives low and high frequency signal. Write 1, the frequency will be disable. Default 0. After power on, the system should set this bit to 1 in order to disable BEEP.

Bit 6: BEEP/GPO# Pin Function Select. Write 1 Select GPO# function. Set 0, select BEEP function. This bit default 0.

Bit 5: FAN 3 output value if FANINC3 sets to 0. Write 1, then pin 18 always generate logic high signal. Write 0, pin 18 always generates logic low signal. This bit default 0.

Bit 4: FAN 3 Input Control. Set to 1, pin 18 acts as FAN clock input, which is default value. Set to 0, this pin 18 acts as FAN control signal and the output value of FAN control is set by this register bit 5. This output pin can connect to power PMOS gate to control FAN ON/OFF.

Bit 3: FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 19 always generate logic high signal. Write 0, pin 19 always generates logic low signal. This bit default 0.

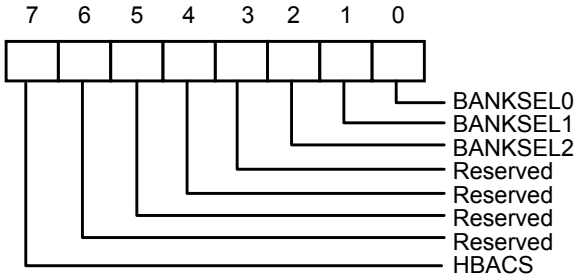
Bit 2: FAN 2 Input Control. Set to 1, pin 19 acts as FAN clock input, which is default value. Set to 0, this pin 19 acts as FAN control signal and the output value of FAN control is set by this register bit 3. This output pin can connect to power NMOS gate to control FAN ON/OFF.

Bit 1: FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 20 always generate logic high signal. Write 0, pin 20 always generates logic low signal. This bit default 0.

Bit 0: FAN 1 Input Control. Set to 1, pin 20 acts as FAN clock input, which is default value. Set to 0, this pin 20 acts as FAN control signal and the output value of FAN control is set by this register bit 1. This output pin can connect to power PMOS gate to control FAN ON/OFF.

8.18 Register 50h ~ 5Fh Bank Select – Index 4Eh (No Auto Increase) (*Bank 0*)

Register Location: 4Eh
Power on Default Value <6:3> = Reserved, <7> = 1, <2:0> = 0. Reset by MR
Attribute: Read/Write
Size: 8 bits



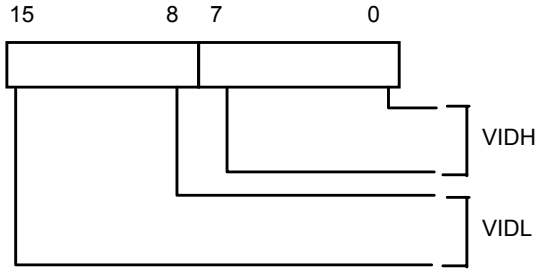
Bit 7: HBACS- High byte access. Set to 1, access Register 4Fh high byte register. Set to 0, access Register 4Fh low byte register. Default 1.

Bit 6-3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

8.19 Winbond Vendor ID – Index 4Fh (No Auto Increase) (*Bank 0*)

Register Location: 4Fh
Power on Default Value <15:0> = 5CA3h
Attribute: Read Only
Size: 16 bits



Bit 15-8: Vendor ID High Byte if CR4E.bit7=1.Default 5Ch.

Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

8.20 Resistor-Temperature Table Register – Index 50h - 51h (Bank 0)

Note: Index will be auto-increased when read Data Port 0x6, and Index will stop at 0x5F if continue reading Data Port. Any no defined register is read will return 0xFF.

A6-A0	NAME	READ/WRITE	DESCRIPTION
50h	RT_IDX	Read/Write	R-T Table index port, which is mapped to data port 51h. The default value is 0x00.
51h	RT_DATA	Read/Write	R-T Table data port, which is selected by RT_IDX.

8.21 Winbond Test Register 1 – Index 52h (Bank 0)

Reserved

8.22 Winbond Test Register 2 – Index 53h (Bank 0)

Reserved

8.23 Winbond Test Register 3 – Index 54h (Bank 0)

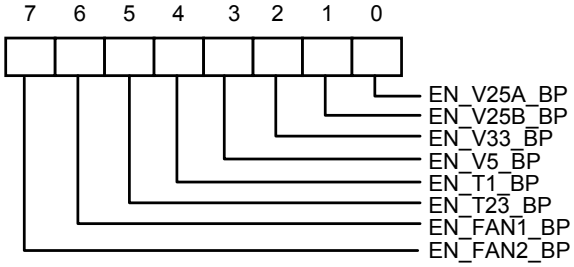
Reserved

8.24 Winbond Test Register 4 – Index 55h (Bank 0)

Reserved

8.25 BEEP Control Register 1 – Index 56h (*Bank 0*) (Auto-increment)

Register Location: 56h
Power on Default Value <7:0> 0000,0000. Reset by MR.
Attribute: Read/Write
Size: 8 bits



Bit 7: Enable BEEP Output from FAN 2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default value is 0.

Bit 6: Enable BEEP Output from FAN 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default value is 0.

Bit 5: Enable BEEP Output from Temperature Sensor 2 and 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default value is 0.

Bit 4: Enable BEEP output for Temperature Sensor 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default value is 0.

Bit 3: Enable BEEP output from VDD (5V), Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 2: Enable BEEP output from 3.3V. Write 1, enable BEEP output. Default value is 0.

Bit 1: Enable BEEP output from V-Core B. Write 1, enable BEEP output. Default value is 0.

Bit 0: Enable BEEP Output from V-Core A if the monitor value exceed the limits value. Write 1, enable BEEP output. Default value is 0.

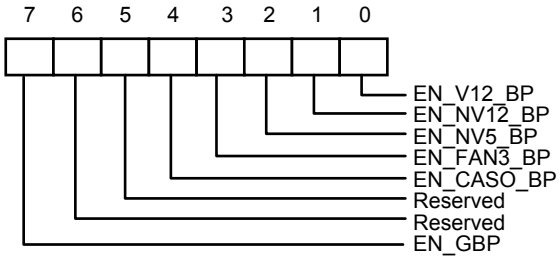
8.26 BEEP Control Register 2 – Index 57h (*Bank 0*) (No Auto-increment)

Register Location: 57h

Power on Default Value <7:0> 1000-0000. Reset by MR.

Attribute: Read/Write

Size: 8 bits



Bit 7: Enable Global BEEP. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.

Bit 6-5: Reserved. This bit should be set to 0.

Bit 4: Enable BEEP output for case open if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0.

Bit 3: Enable BEEP Output from FAN 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0.

Bit 2: Enable BEEP output from -5V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 1: Enable BEEP output from -12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 0: Enable BEEP output from +12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

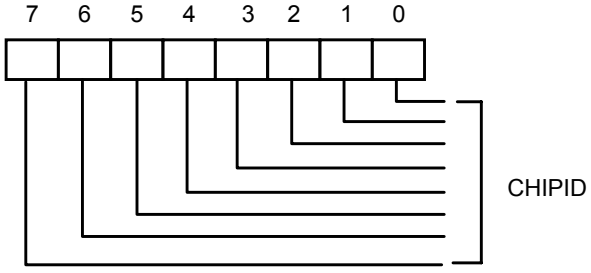
8.27 Chip ID – Index 58h (*Bank 0*)

Register Location: 58h

Power on Default Value <7:0> 0001-0000. Reset by MR.

Attribute: Read Only

Size: 8 bits

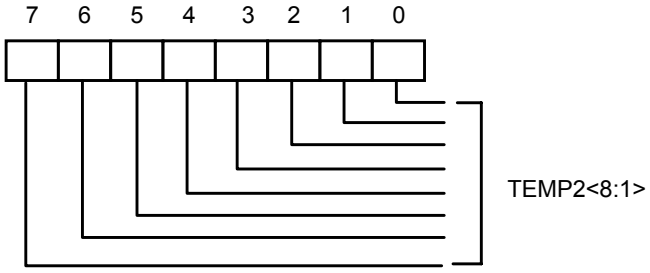


Bit 7: Winbond Chip ID number. Read this register will return 10h.

8.28 Temperature Sensor 2 Temperature Register – Index 50h (*Bank 1*)

Register Location: 50h

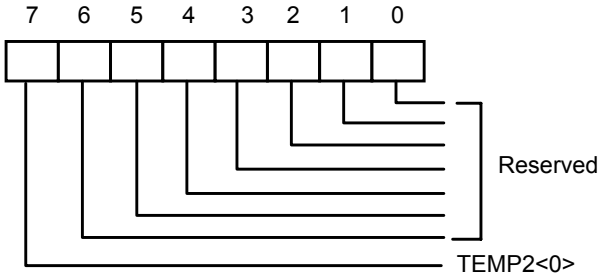
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <8:1> of sensor 2, which is high byte.

8.29 Temperature Sensor 2 Temperature Register – Index 51h (*Bank 1*)

Register Location: 51h
Attribute: Read Only
Size: 8 bits

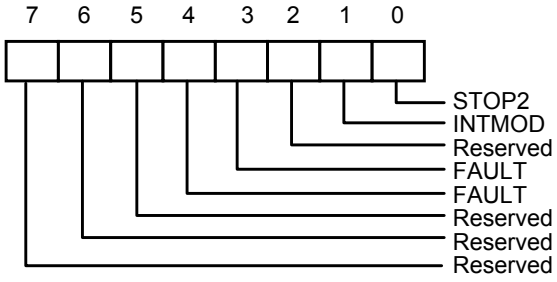


Bit 7: Temperature <0> of sensor2, which is low byte.

Bit 6-0: Reserved. This bit should be set to 0.

8.30 Temperature Sensor 2 Configuration Register – Index 52h (*Bank 1*)

Register Location: 52h
Power on Default Value <7:0> = 0x00
Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

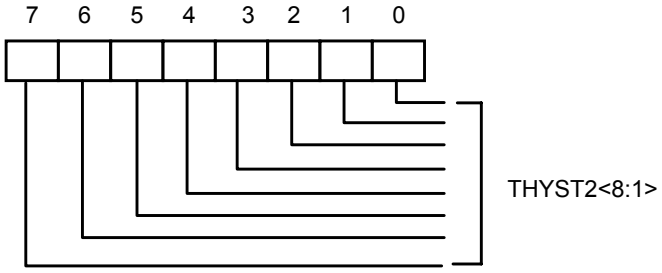
Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - Interrupt mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

8.31 Temperature Sensor 2 Hysteresis (High Byte) Register – Index 53h (*Bank 1*)

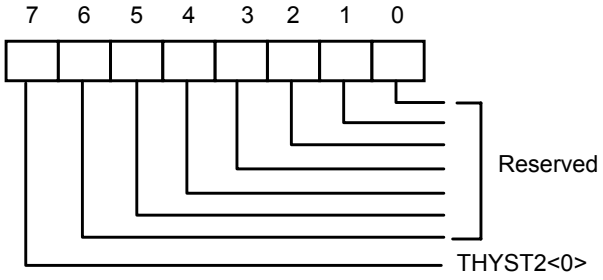
Register Location: 53h
Power on Default Value <7:0> = 0x4B
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

8.32 Temperature Sensor 2 Hysteresis (Low Byte) Register – Index54h (*Bank 1*)

Register Location: 54h
Power on Default Value <7:0> = 0x0
Attribute: Read Only
Size: 8 bits

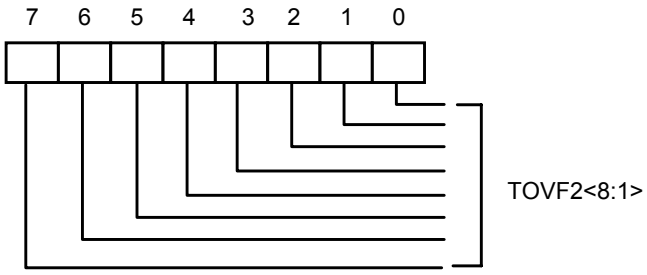


Bit 7: Temperature hysteresis bit 0, which is low Byte.

Bit 6-0: Reserved. This bit should be set to 0.

8.33 Temperature Sensor 2 Over-temperature(High Byte) Register – Index 55h (*Bank 1*)

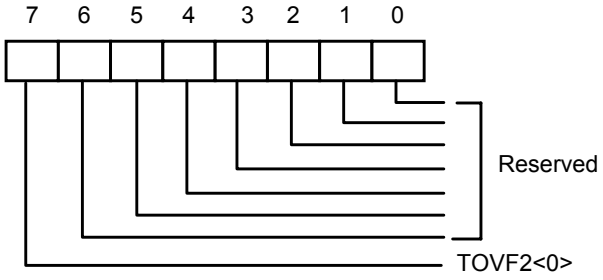
Register Location: 55h
Power on Default Value <7:0> = 0x50
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

8.34 Temperature Sensor 2 Over-temperature (Low Byte) Register – Index 56h (*Bank 1*)

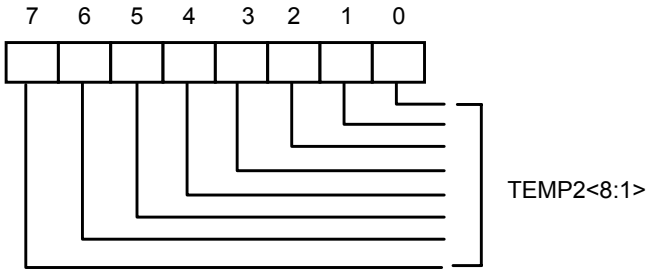
Register Location: 56h
Power on Default Value <7:0> = 0x0
Size: 8 bits



Bit 7: Read/Write - Over-temperature bit 0, which is low Byte.
Bit 6-0: Read Only - Reserved. This bit should be set to 0.

8.35 Temperature Sensor 3 Temperature Register - Index 50h (*Bank 2*)

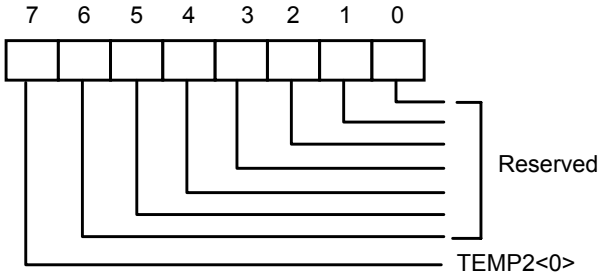
Register Location: 50h
Attribute: Read Only
Size: 8 bits



Bit 7-0: Temperature <8:1> of sensor 2, which is high byte.

8.36 Temperature Sensor 3 Temperature Register – Index 51h (Bank 2)

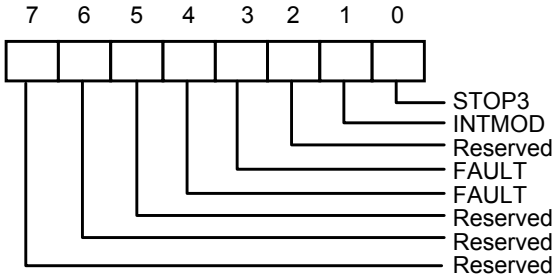
Register Location: 51h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <0> of sensor2, which is low byte.
Bit 6-0: Reserved. This bit should be set to 0.

8.37 Temperature Sensor 3 Configuration Register – Index 52h (*Bank 2*)

Register Location: 52h
Power on Default Value <7:0> = 0x00
Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVF# output to avoid false tripping due to noise.

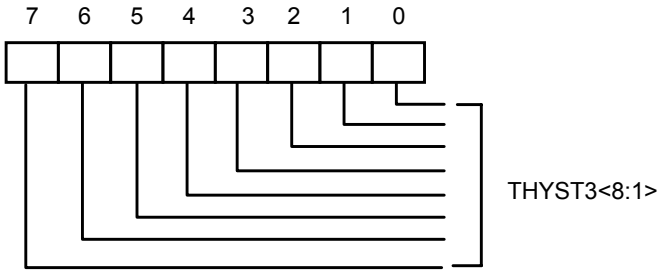
Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - Interrupt Mode select. This bit default is set to 0, which is Compared Mode. When set to 1, Interrupt Mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

8.38 Temperature Sensor 3 Hysteresis (High Byte) Register – Index 53h (Bank 2)

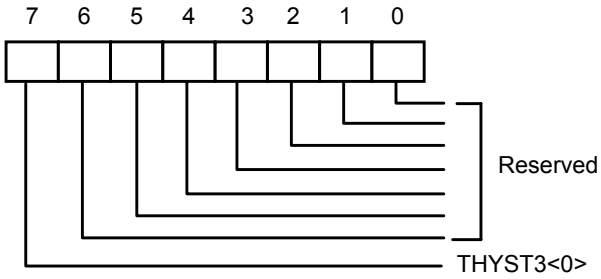
Register Location: 53h
Power on Default Value <7:0> = 0x4B
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

8.39 Temperature Sensor 3 Hysteresis (Low Byte) Register – Index 54h (*Bank 2*)

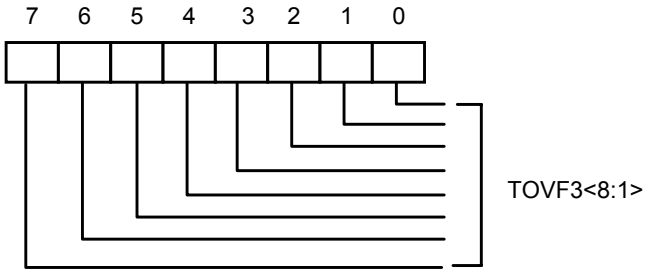
Register Location: 54h
Power on Default Value <7:0> = 0x0
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature hysteresis bit 0, which is low Byte.
Bit 6-0: Reserved. This bit should be set to 0.

8.40 Temperature Sensor 3 over temperature (High Byte)Register – Index 55h (*Bank 2*)

Register Location: 55h
Power on Default Value <7:0> = 0x50
Attribute: Read/Write
Size: 8 bits



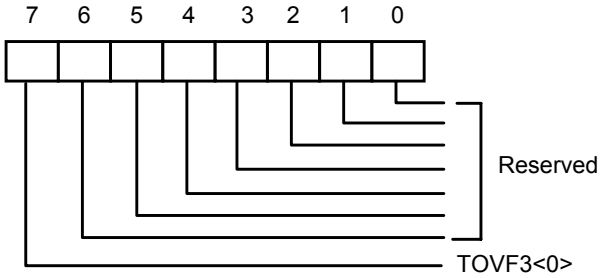
Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

8.41 Temperature Sensor 3 Over-temperature (Low Byte) Register – Index 56h (*Bank 2*)

Register Location: 56h

Power on Default Value <7:0> = 0x0

Size: 8 bits



Bit 7: Read/Write - Over-temperature bit 0, which is low Byte.

Bit 6-0: Read Only - Reserved. This bit should be set to 0.

9. ELECRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 5V ± 10%, VSS = 0V)

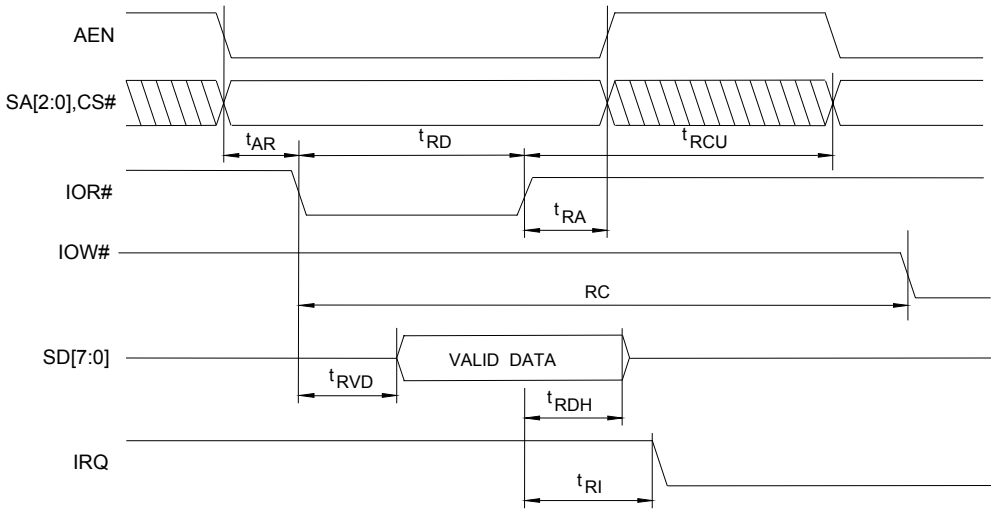
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA

DC Characteristics, continued

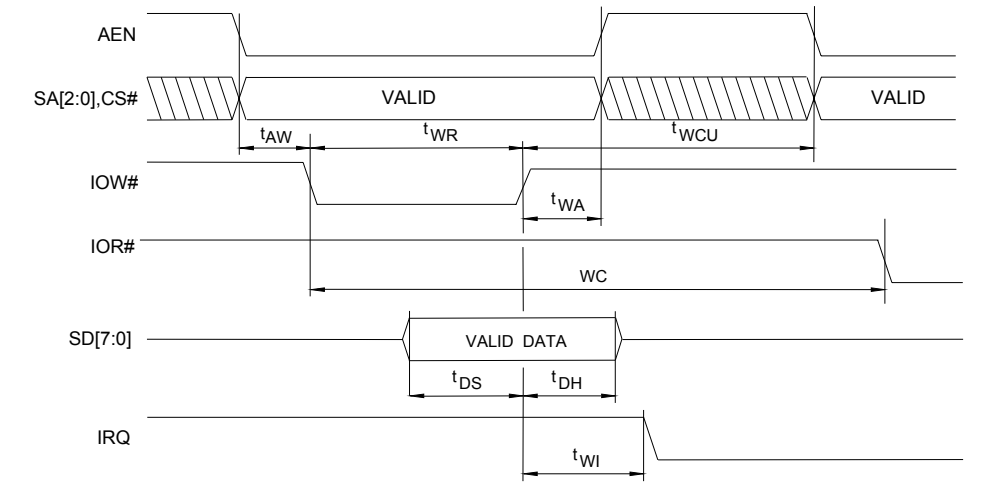
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

9.3 AC Characteristics

9.3.1 ISA Read/Write Interface Timing



ISA Bus Read Timing

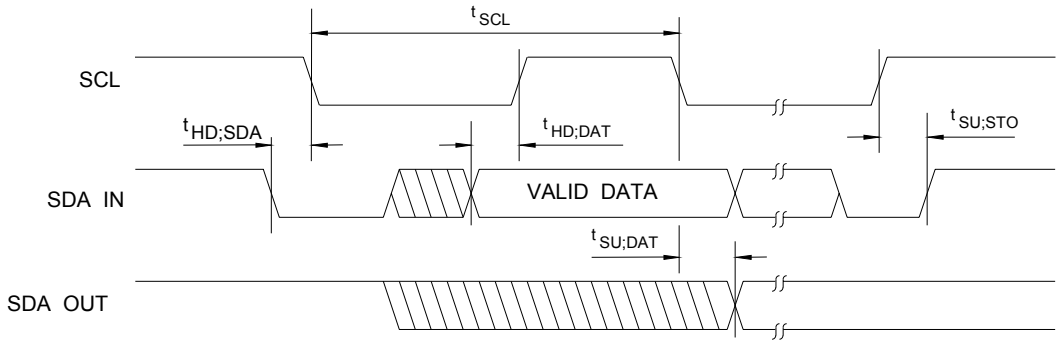


ISA Bus Write Timing

ISA Read/Write Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Valid Address to Read Active	t_{AR}	10		nS
Valid Address to Write Active	t_{AW}	10		nS
Data Hold	t_{DH}	5		nS
Data Setup	t_{DS}	80		nS
Address Hold from Inactive Read	t_{RA}	40		nS
Read Cycle Update	t_{RCU}	200		nS
Read Strobe Width	t_{RD}	120		nS
Read Data Hold	t_{RDH}	40		nS
Read Strobe to Clear IRQ	t_{RI}		60	nS
Active Read to Valid Data	t_{RVD}		115	nS
Address Hold from Inactive Write	t_{WA}	5		nS
Write Cycle Update	t_{WCU}	80		nS
Write Strobe to Clear IRQ	t_{WI}		60	nS
Write Strobe Width	t_{WR}	120		nS
Read Cycle = $t_{AR} + t_{RD}+t_{RCV}$	RC	330		nS
Write Cycle = $t_{AW}+t_{WR}+t_{WCV}$	WC	210		nS

9.3.2 Serial Bus Timing Diagram



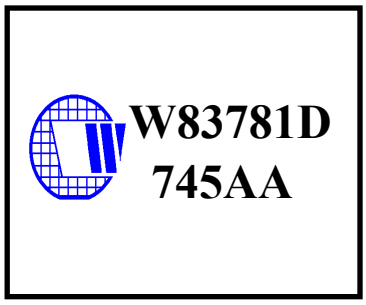
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL Clock Period	t_{SCL}	10		uS
Start Condition Hold Time	$t_{HD;SDA}$	4.7		uS
Stop Condition Setup-up Time	$t_{SU;STO}$	4.7		uS
DATA to SCL Setup Time	$t_{SU;DAT}$	120		nS
DATA to SCL Hold Time	$t_{HD;DAT}$	5		nS
SCL and SDA Rise Time	t_R		1.0	uS
SCL and SDA Fall Time	t_F		300	nS

10. HOW TO READ THE TOP MARKING

The top marking of W83781D

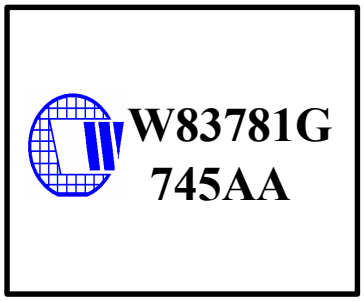


Left: Winbond logo

1st line: Type number W83781D, D means LQFP (Thickness = 1.4 mm).
2nd line: Tracking code 745 A A

745: packages made in '97, week 45
A: assembly house ID; A means ASE, O means OSE
A: IC revision; A means version A, B means version B

The top marking of W83781G



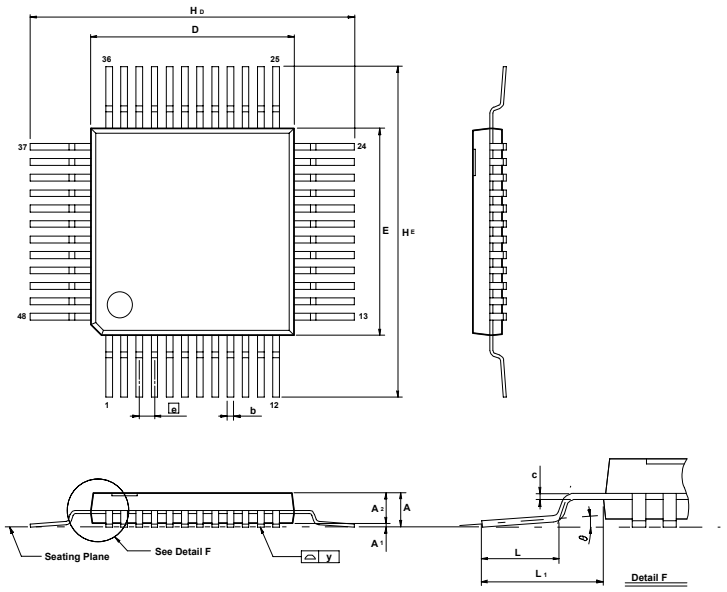
Left: Winbond logo

1st line: Type number W83781G, G means lead-free package.
2nd line: Tracking code 745 A A

745: packages made in '97, week 45
A: assembly house ID; A means ASE, O means OSE
A: IC revision; A means version A, B means version B

11. PACKAGE DIMENTIONS

(48-pin QFP)

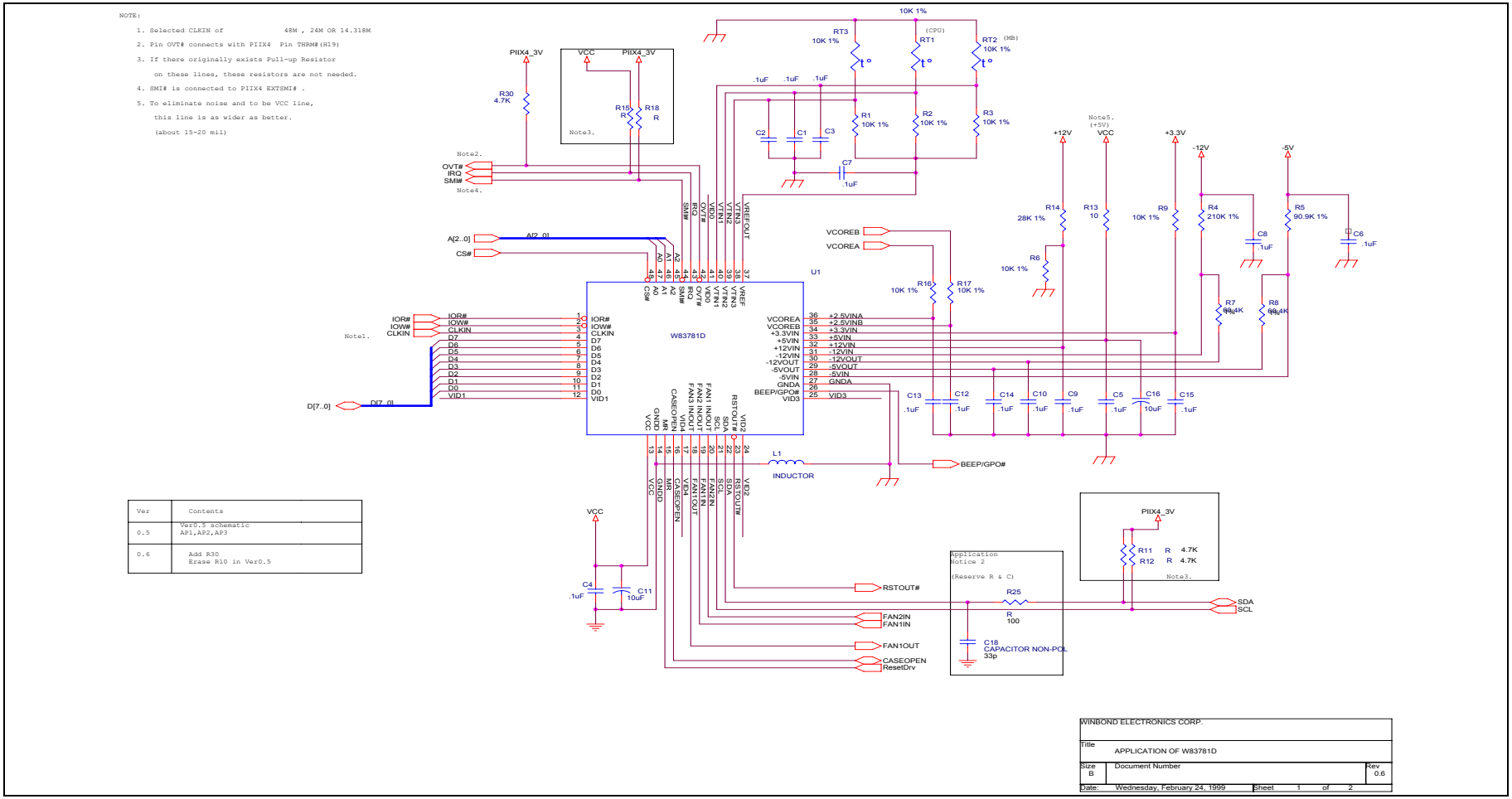


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

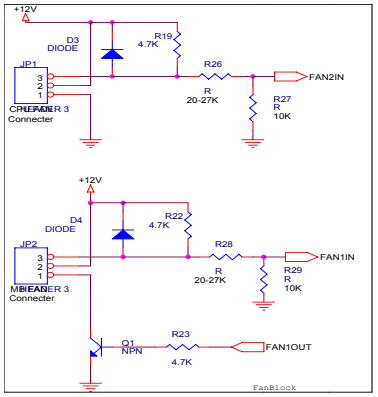
Notes:

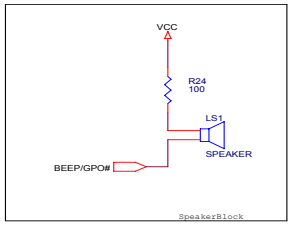
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

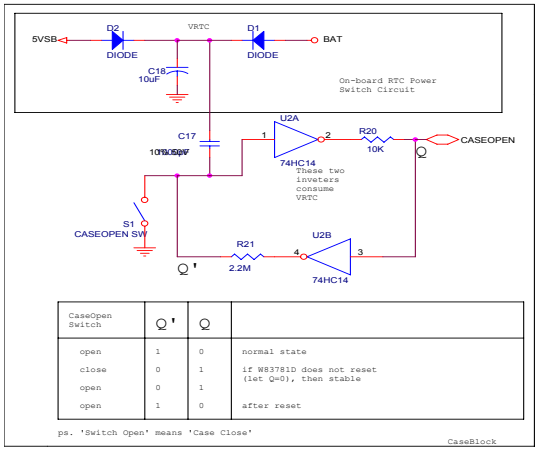
12. APPLICATION CIRCUITS OF W83781D



Ver	Contents
0.5	Ver0.5 schematic AP1,AP2,AP3
0.6	Add R30 Erase R10 in Ver0.5







WINBOND ELECTRONICS CORP.			
Title	APPLICATION OF W83781D		
Size B	Document Number		Rev 0.6
Date: Wednesday, February 24, 1999	Sheet 2 of 2		

REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
		n.a.	All the version before 0.60 are internal use.
0.60	11/07/97	n.a.	First published.
0.61	11/19/97	5	Pin 18-20: I/O Type → I/O_{12ts}
0.62	12/17/97	4 5 6	Pin18-20:I/O Type → Fan 1, Pin18:Fan1→ Fan3 Pin23: I/O Type → OUT_{8t} Pin42: I/O Type → OUT_{12}
0.63	1/13/98	33 37 40 43 48	8.24 index 55h(Bank 0) → Winbond Test Register 8.30 index 52h(Bank 1) bit2 → Reserve 8.37 index 52h(Bank 2) bit2 → Reserve 9.2 I/O 12ts TTL DC Characteristics Package QFT → LQFP
0.64	05/19/98	13	Divisor table 1, 2, 3, 4 → 1, 2, 4, 8
1.0	04/11/02	n.a.	Change all version include version on web site to 1.0
1.1	10/25/02	48	Verify ISA Bus RD Timing. (210 =>330ns)
1.2	01/06/05	n.a.	Lead-free package version
2.0	April 14, 2005	48	ADD Important Notice

Important Notice

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